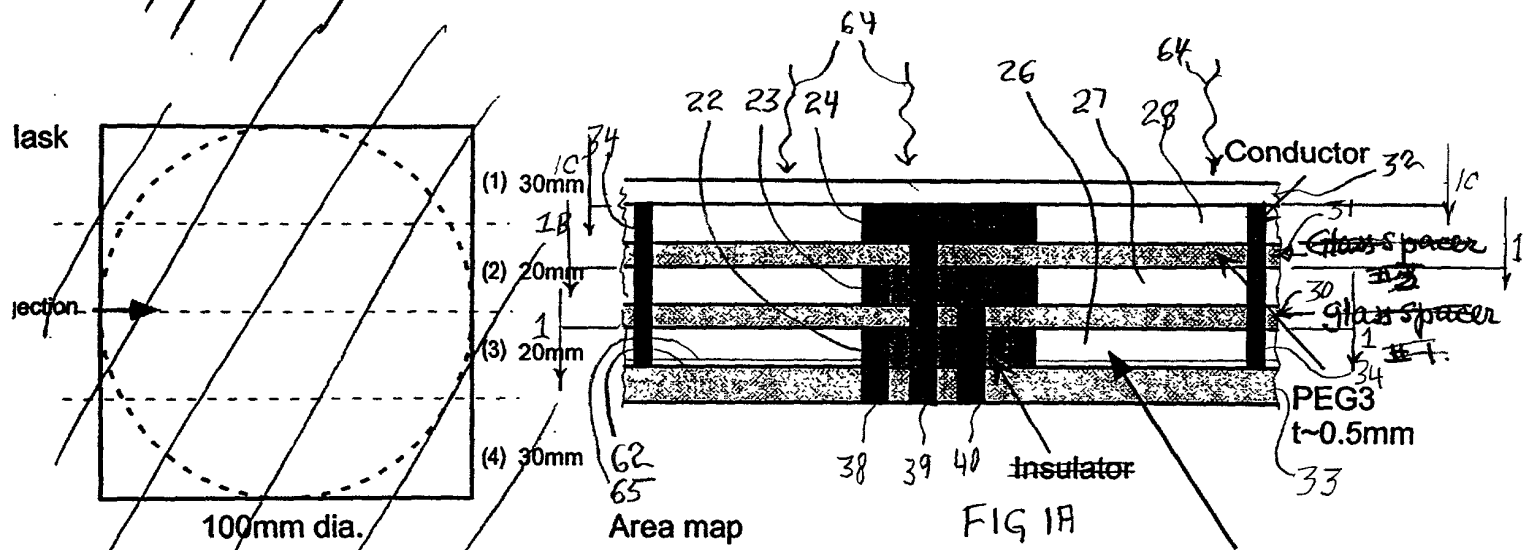


Layer #1



This layer

- (1) Unit cell size 350 μm
- (2) Unit cell size 250 μm
- (3) Unit cell size 300 μm
- (3) Unit cell size 400 μm

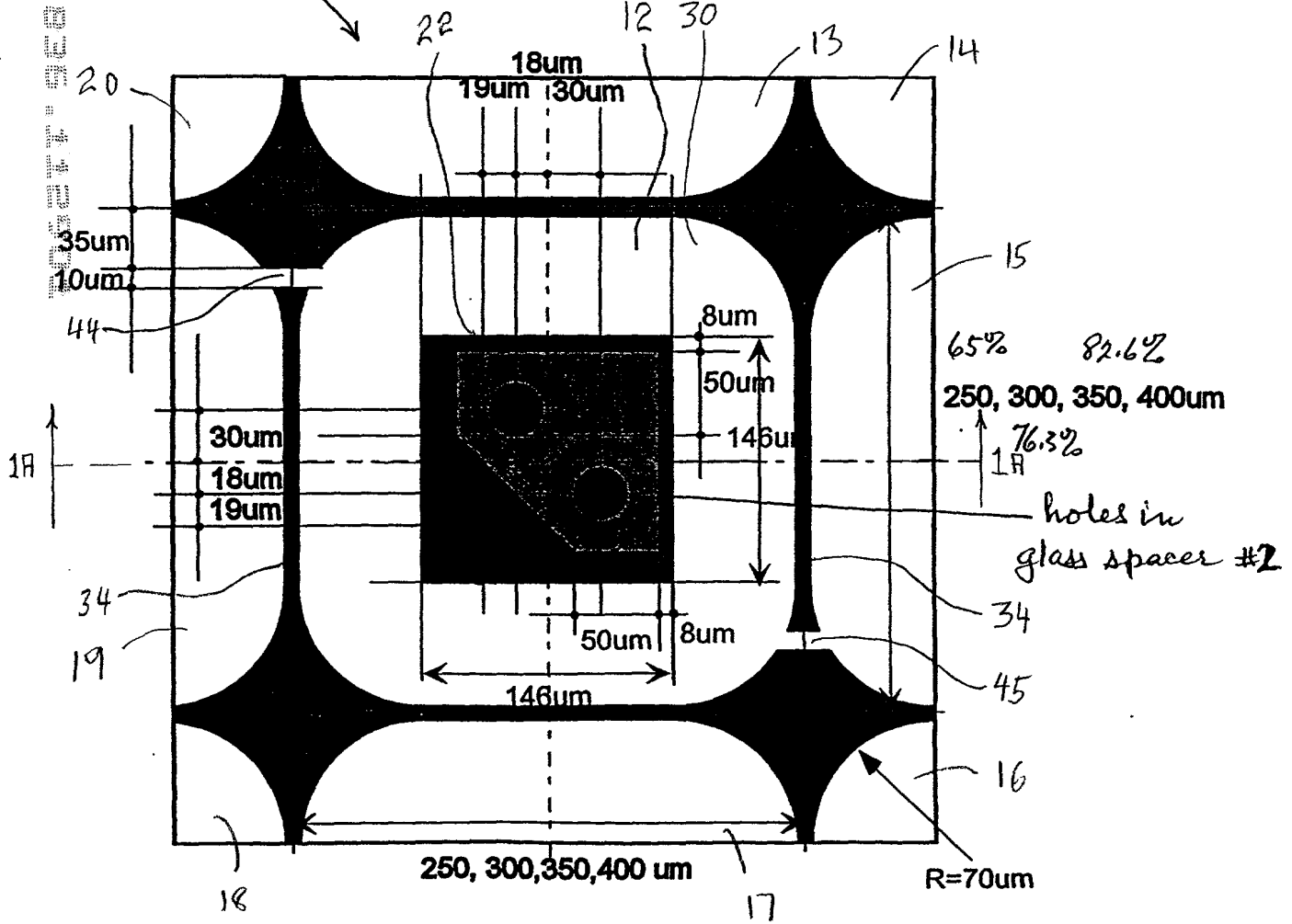


Figure 1

Layer #2

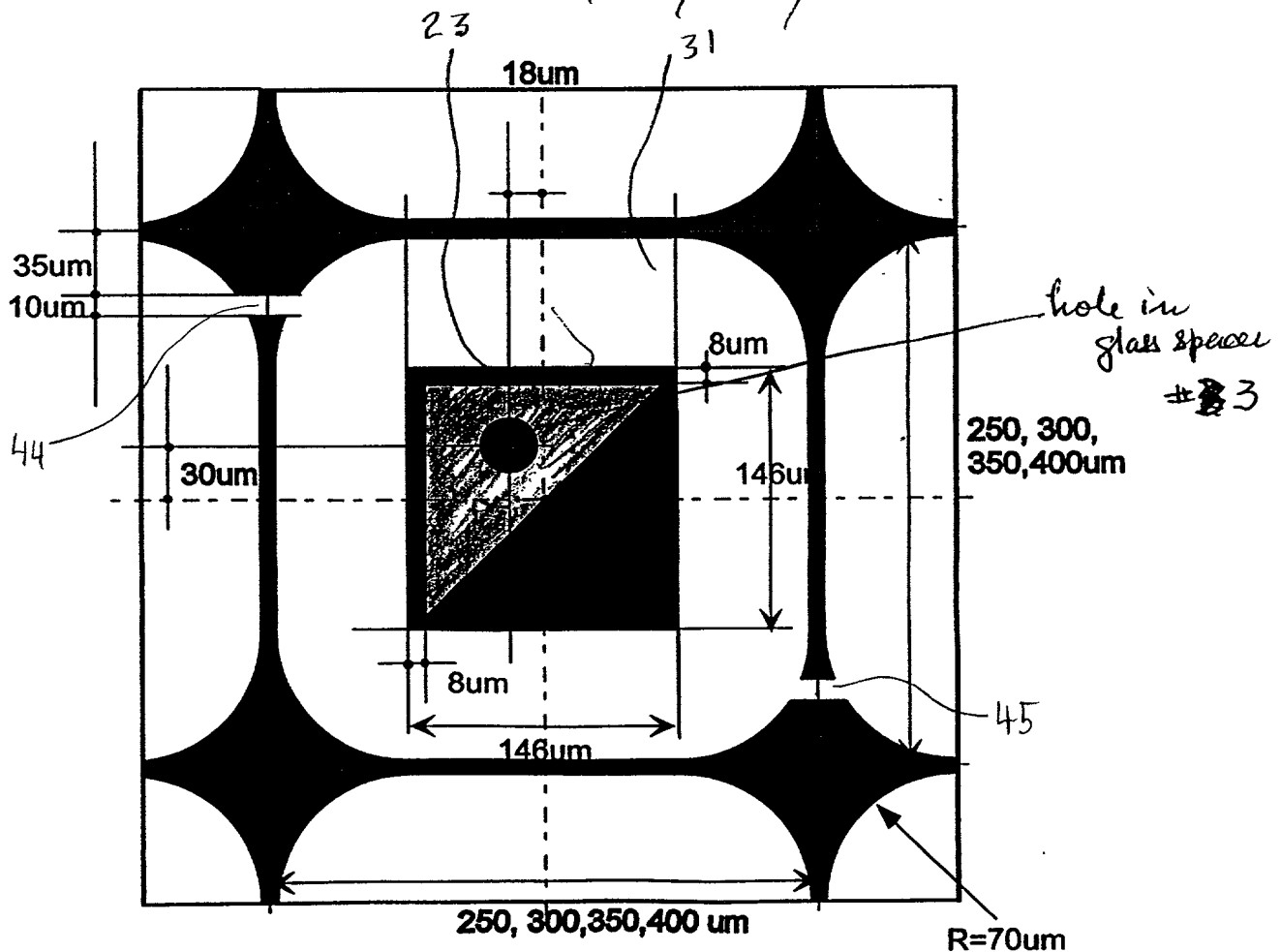
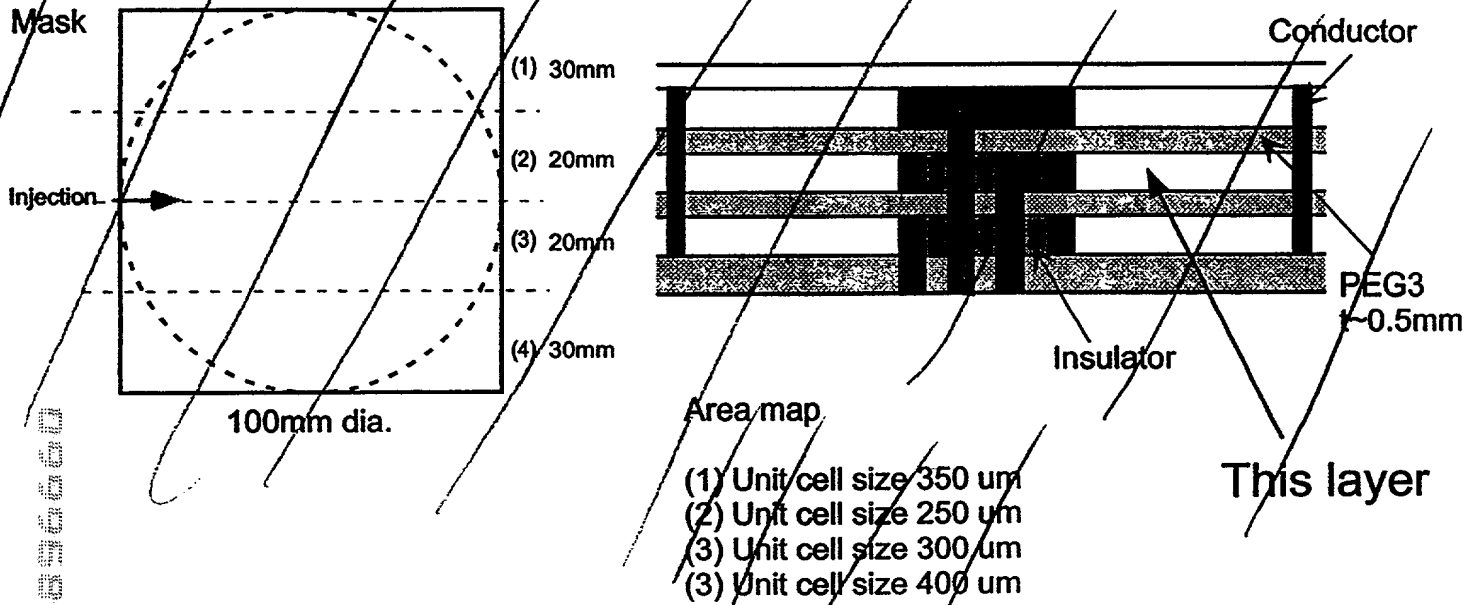


Figure 1 B

Layer #3

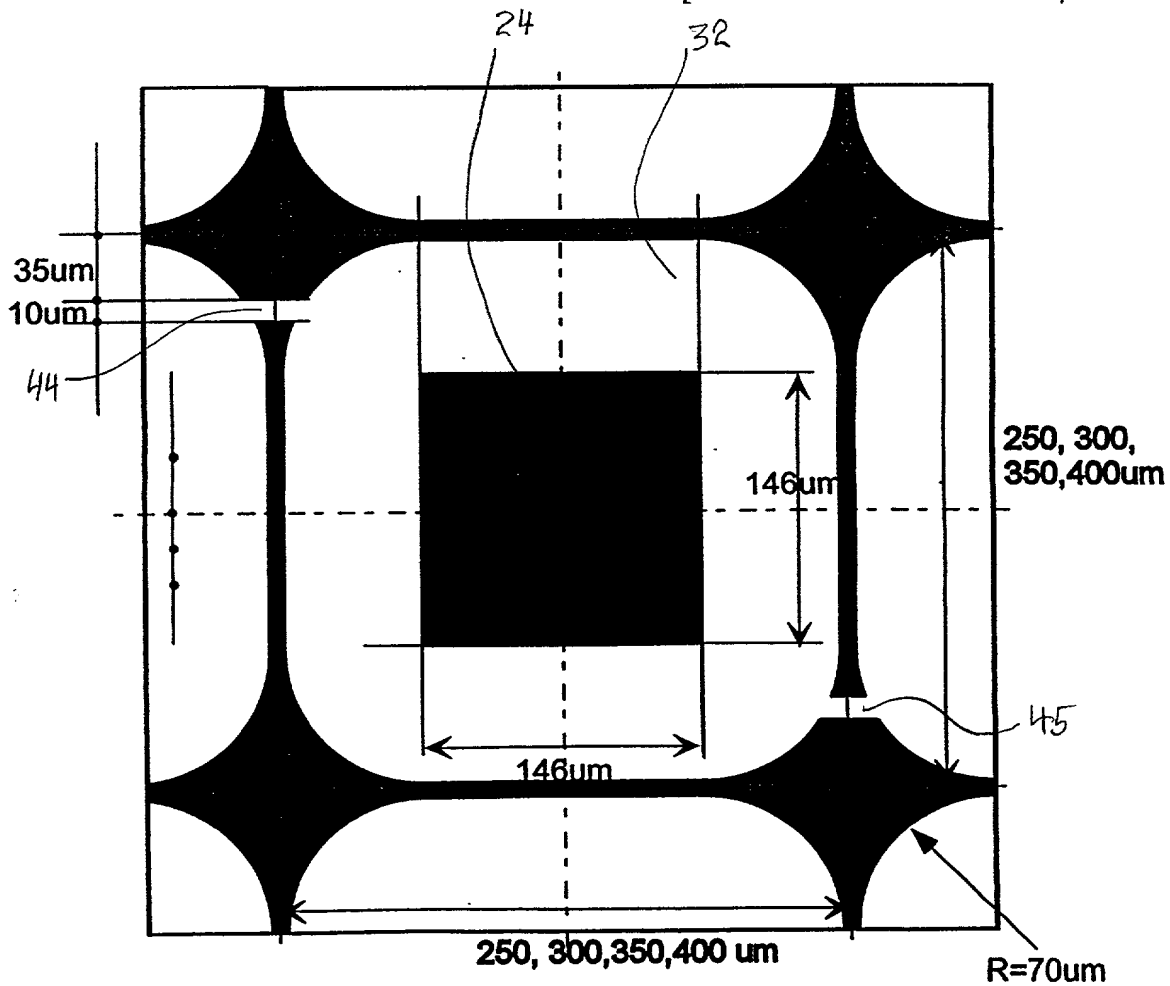
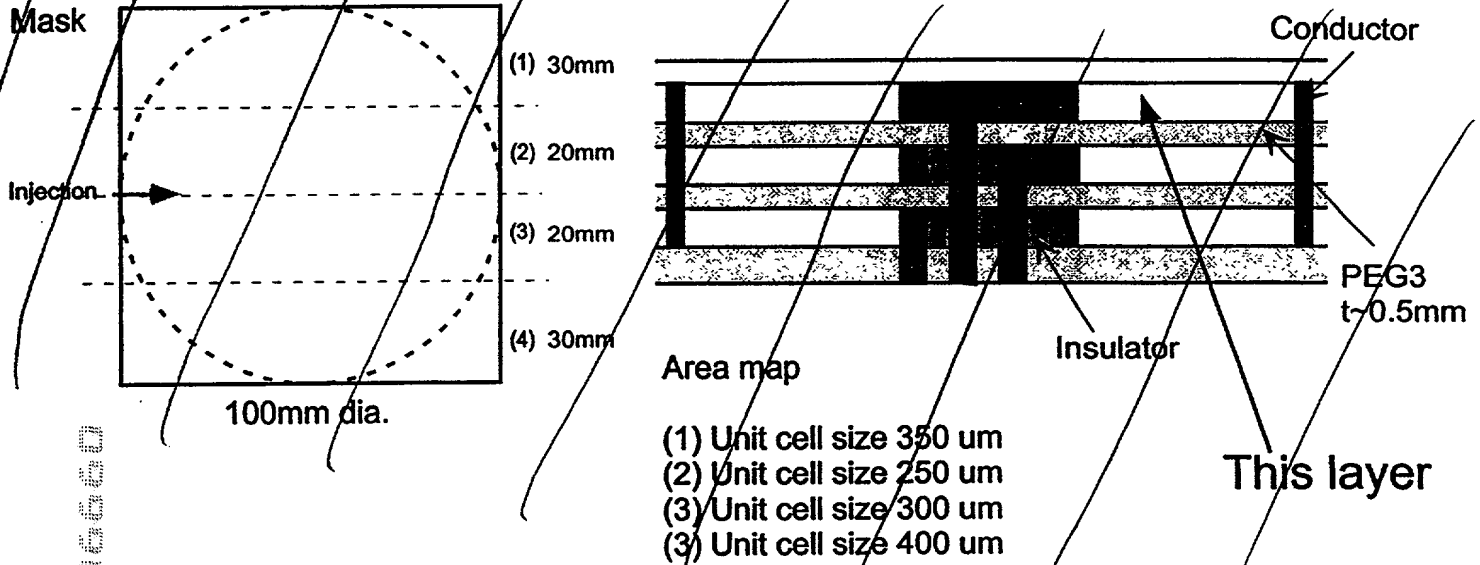


Figure 1 C

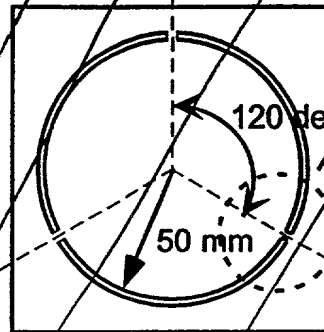
PEG process mask #4 (Cover grass mask, this is irradiated opposite side)

All dimension in masks for PEG processing
should be enlarged by 1.0005 times. Reversal

Area map

- (1) Unit cell size 350 um
- (2) Unit cell size 250 um
- (3) Unit cell size 300 um
- (3) Unit cell size 400 um

5 in. sq. quartz substrate

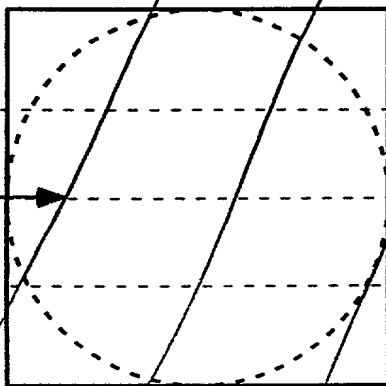


1mm

2mm

Mask

Injection



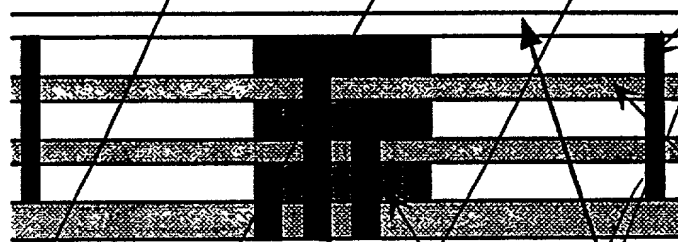
(1) 30mm

(2) 20mm

(3) 20mm

(4) 30mm

100mm dia.

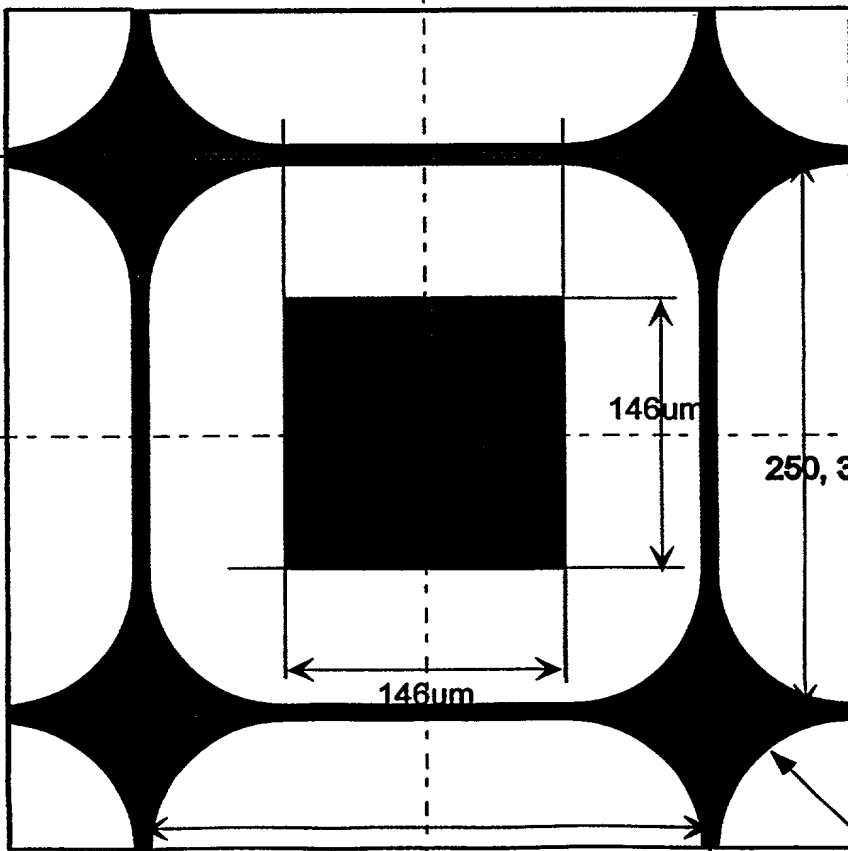


Conductor

Insulator

PEG3
t=0.5mm

This Grass



146um

250, 300, 350, 400um

146um

250, 300, 350, 400 um

R=70um

Figure 1D.

Fabrication Process

- 1. Via in layer substrate
- 2. ITO
- 3. Vertical electrode for layer joining
- 4. Polyimide coat
- 5. Layer joining

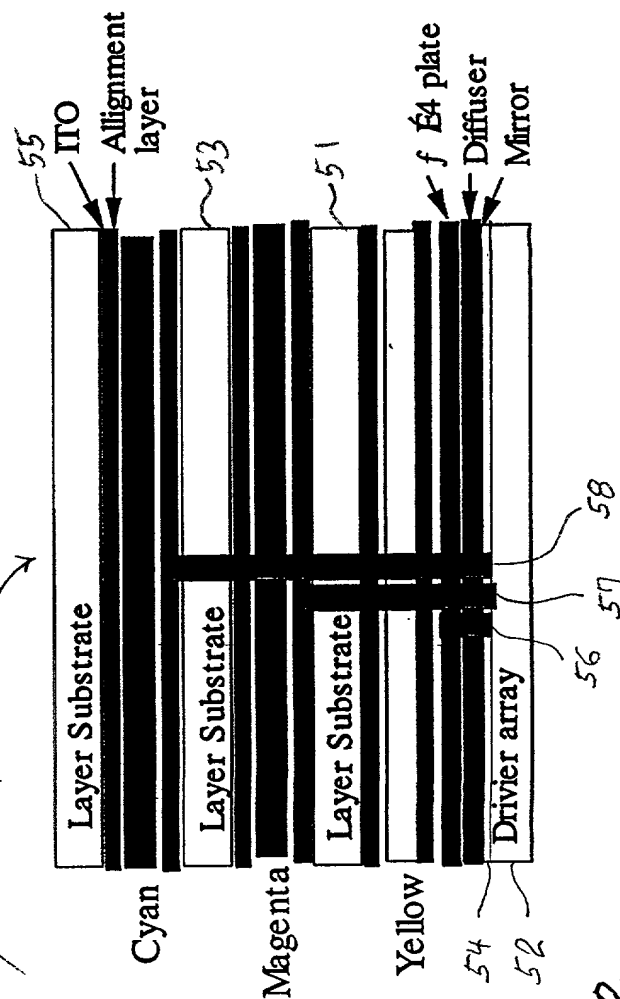


Figure 2.

Cover glass

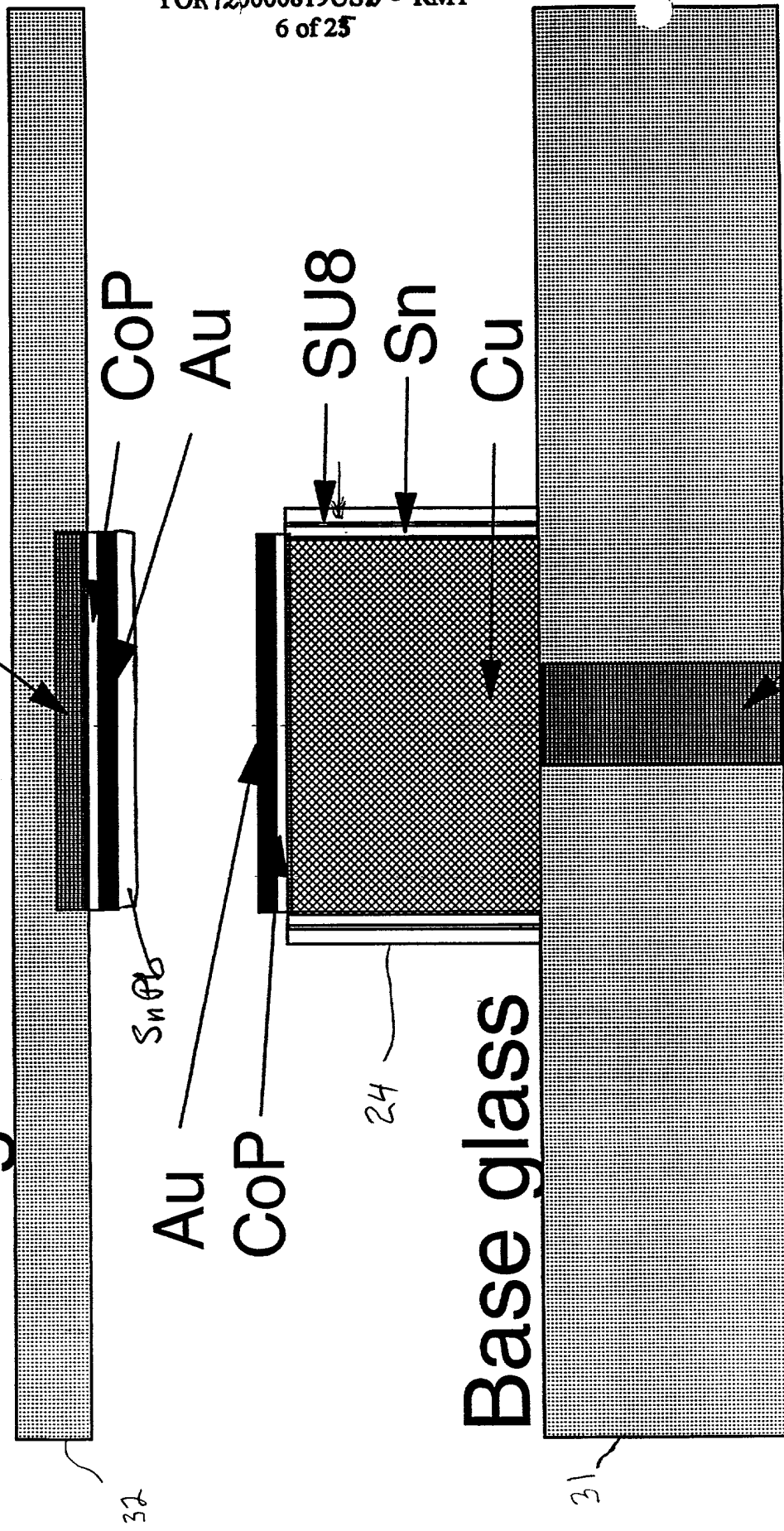


Figure 3

Schematic of joining metallurgy

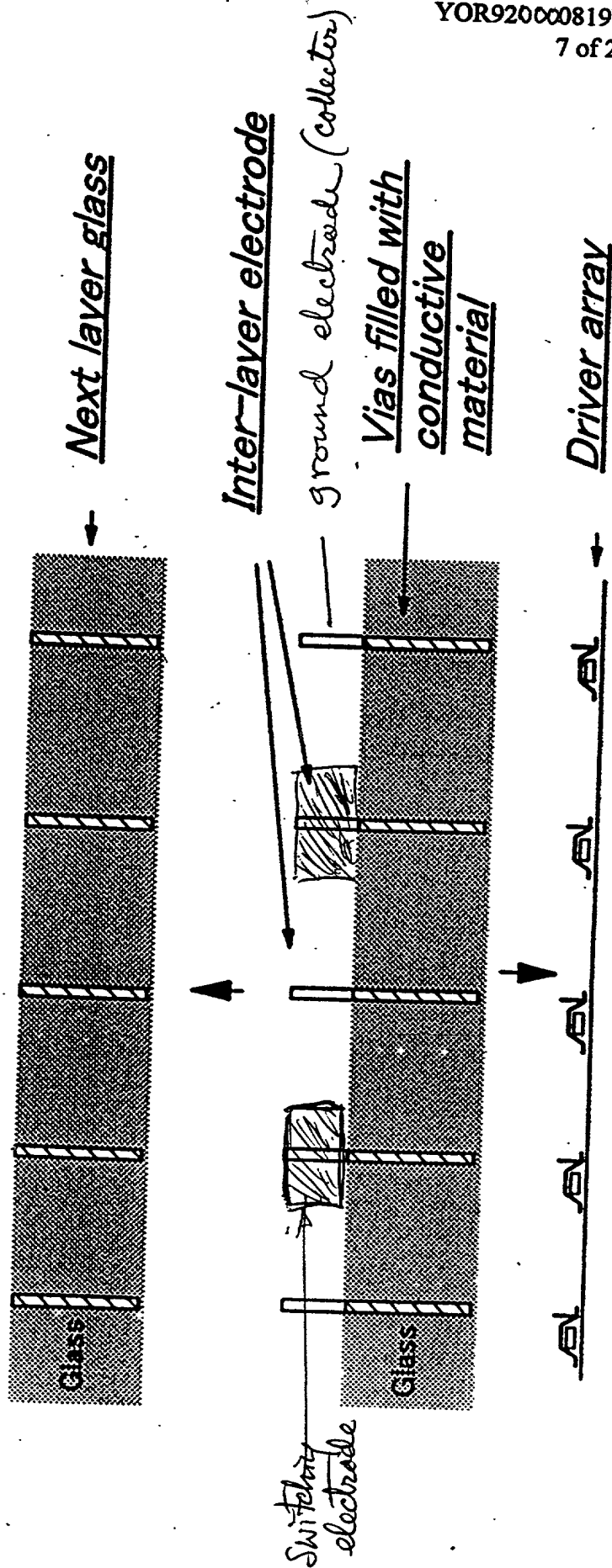


Figure 2. Vertical electrical connection fabrication

process. Figure 4(A) Multilayered stacked structure before final assembly

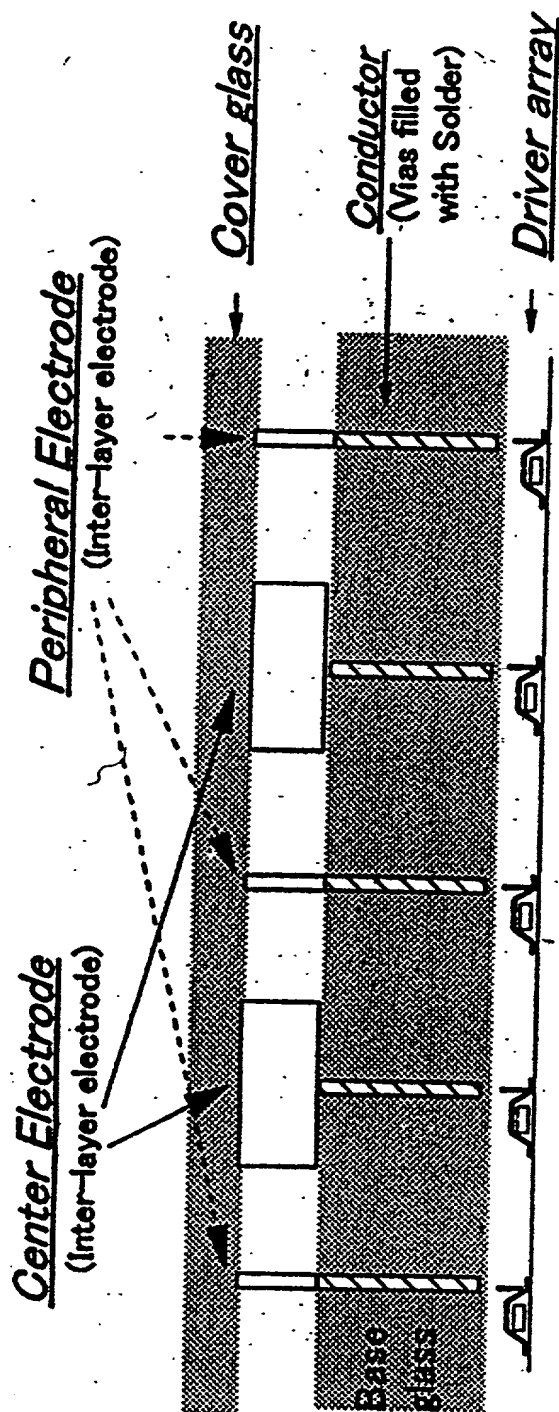
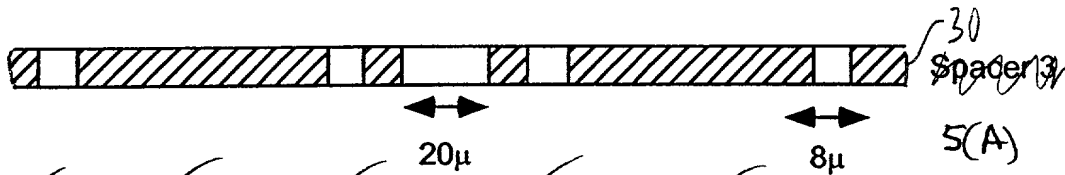


Figure 7. Side view of a one-layer electrophoretic display.

Figure 4(B) A completed one layer electrophoretic display structure

Figure 5

FABRICATION OF GLASS SPACERS #2 & #3



(1) Glass substrate with holes as shown in figure 2 and in this figure the glass will be Hoya photosensitive type glass. Glass substrate will be purchased from a Hoya Glass with the holes already produced in it.

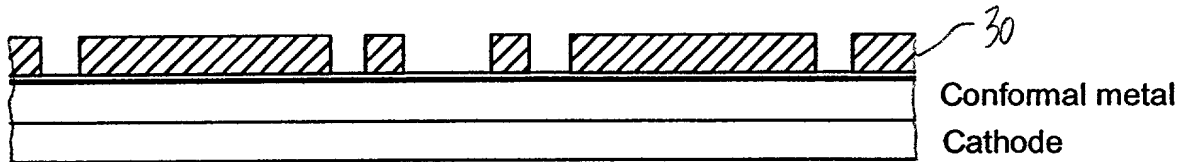


Figure 5(B)

(2) Glass is pressed against a conformal substrate such as metal filled epoxy, elastic polymer with a thin foil of gold, or stainless steel foil.



Figure 5(C)

(3) During electroplating metal is allowed to overplate.

(4) The overplated metal is removed by CMP. The planarized substrate still attached to the metal carrier will be processed further see figure 1.

(5) The planarized metal filled glass will be sputtered with 200 Å Ti and 800 Å Cu (200 Å Ti and 1000 Å Ni, if we decide to use Ni metallurgy)

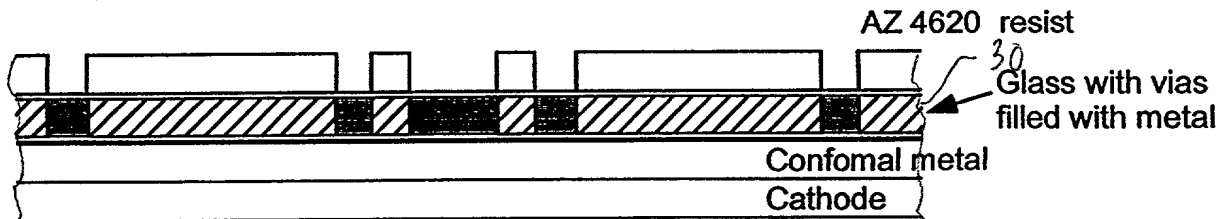


Figure 5(D)

(6) The planarized metal filled glass substrate still attached to the cathode will be spun on with 10 to 12 μm of AZ 4620 resist

(7) After mask alignment with the metal filled vias, AZ-4620 will be exposed and developed - opening the metal

(8) 10 to 15 μm of copper or nickel will be electroplated.

- (9) The resulting Copper/AZ Resist or Ni/AZ Resist structure will be polished to planarize
- (10) 2000 to 5000 Å of SnBi or Sn Pb (eutectic – low temperature) will be electroplated
- (11) AZ resist will be removed by exposure and development.
- (12) The seed layer of Cu will be electroetched followed by 0.1 % HF chemical etch of Ti, or will be sputter etched.
- (13) A layer of SU8 epoxy based negative working resist will be applied and cured.
- (14) The epoxy resist will be planarized sufficiently to expose electroplated SnPb or SnBi.
- (15) A mask will be exposed and developed resulting in structure shown below.

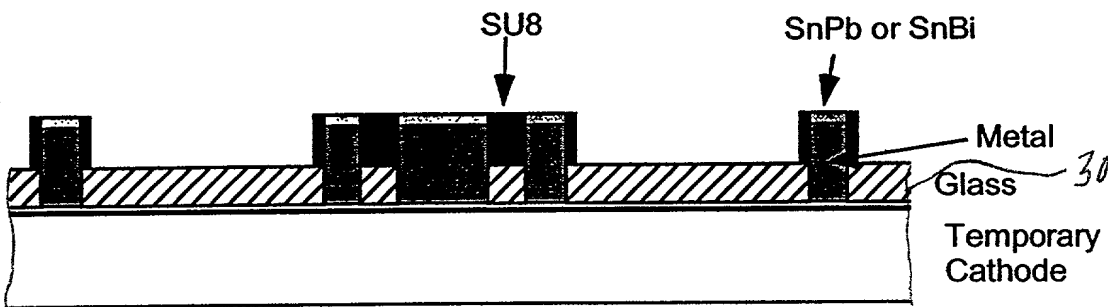


Fig. 5 (E)

- (16) After removal of the glass from the substrate (cathode carrier) the parts will be dipped into electroless Sn or In solution to overcoat the metal by a thin solder (backside).
- (17) When all parts are completed they will be aligned clamped and heated. When temperature of melting of solder is reached the clamp will be released and heating will continue for 30 minutes to permit all cells to self align. A slight amount of vibration may be necessary for plate to move until self aligned. The assembly will then be cooled.
- (18) The part will now be ready to be filled with the electrophoretic solution.

While the masks should be made for all levels at the same time it should be possible to prove the concept by building only the top compartments and the cover glass. Upon assembly this will represent a monochrome display. If the concept works further levels can then be fabricated and the total structure can be built on a glass equipped with TFT's.

Top Cover Plate - Top View

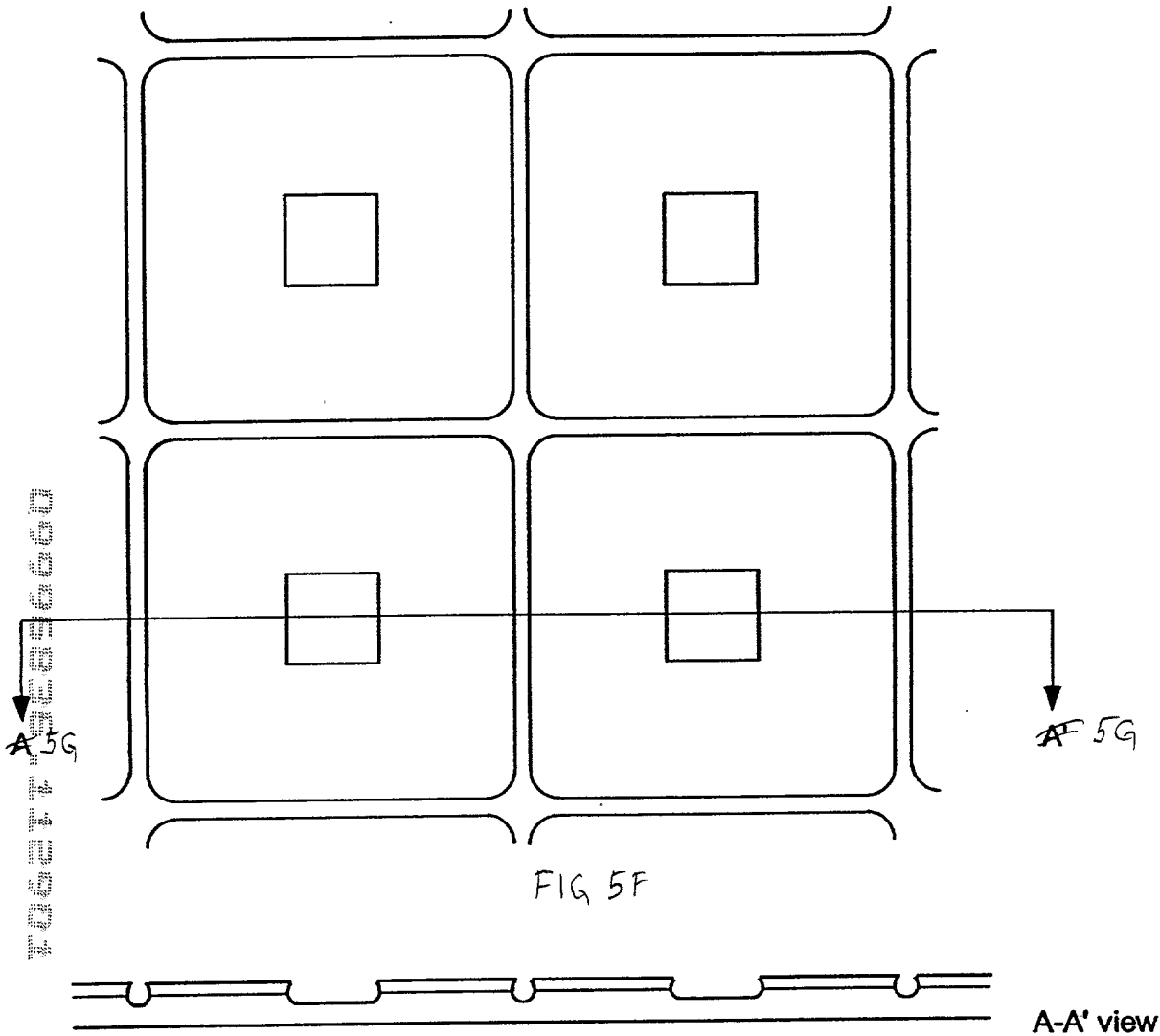


FIG 5F

FIG 5G

~~Figure 5~~ ~~Figure 5(F)~~

- (1) Glass will be coated with AZ 4620 resist and exposed with a pattern shown above with slight overhang.
- (2) Glass will be etched in 500 A deep with HF.
- (3) After rinsing it will be sputtered with 500 A of Ni or Ti and lift-off will be performed.
- (3) a) Alternatively and electroless Ni will be plated into the grooves. The plated Ni will be overcoated by thin Sn or In by plating.

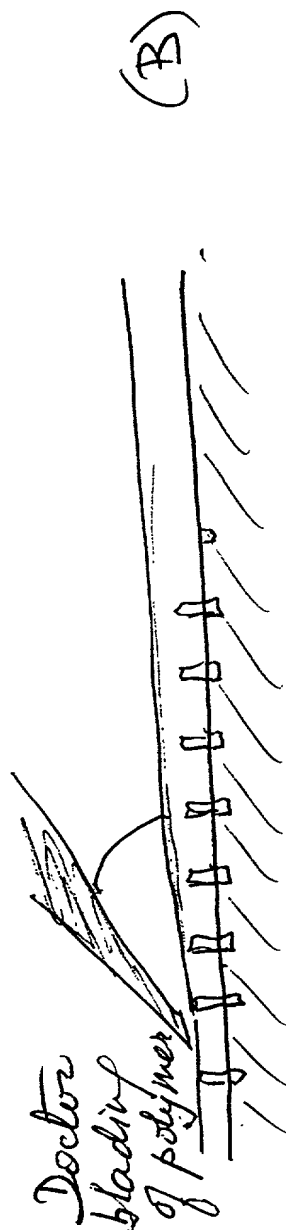
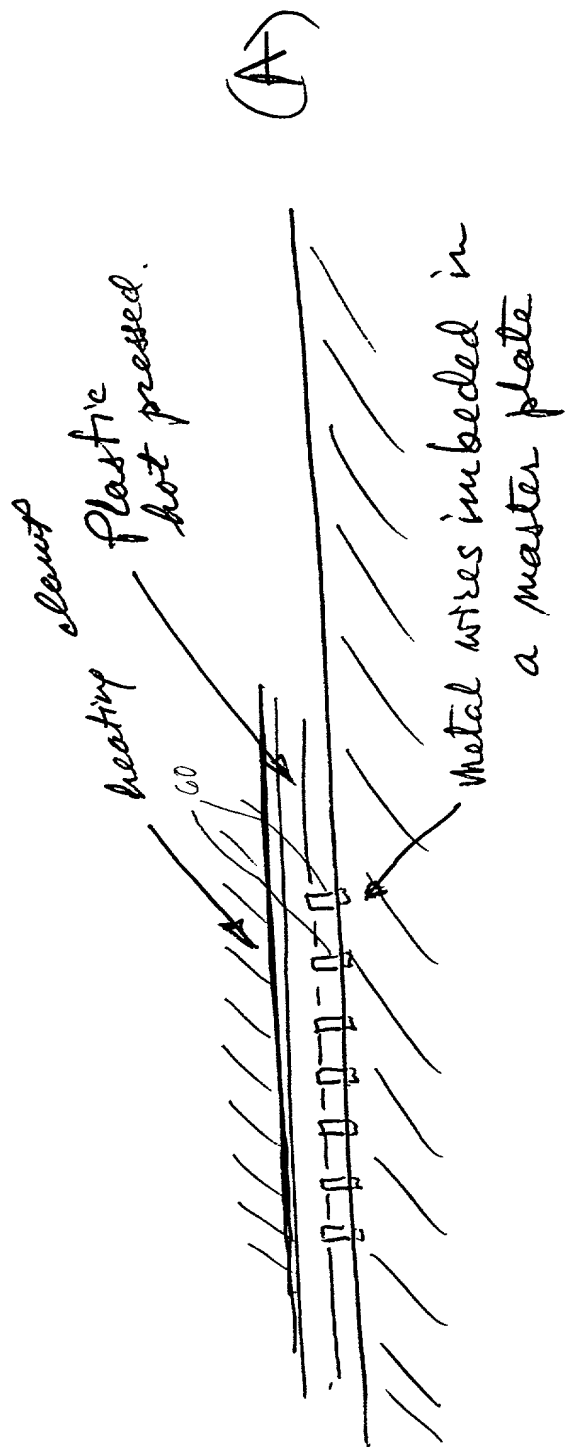
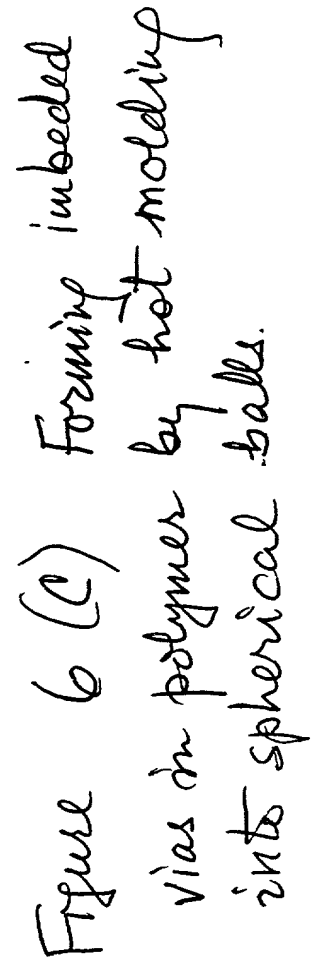
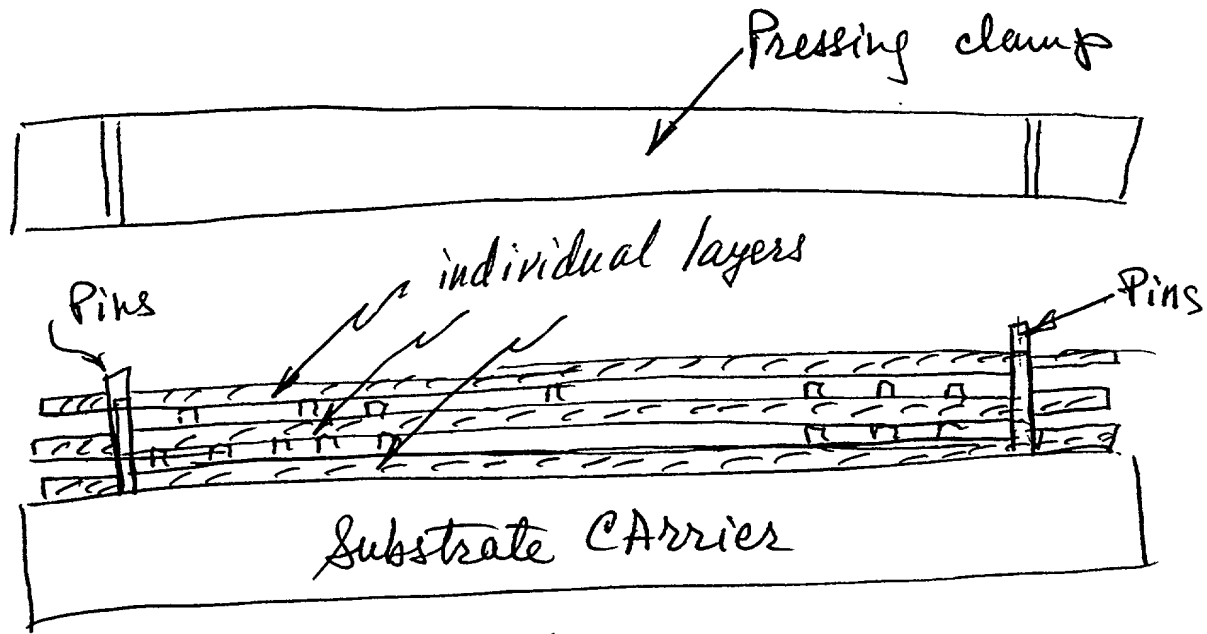


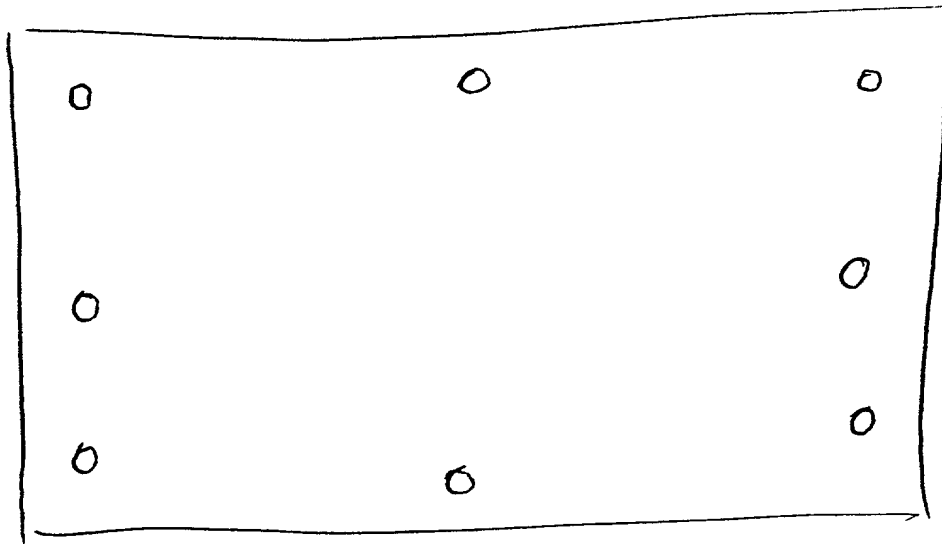
Figure 6 (A) Forming ^{metal} vias in polymer by hot pressing and moulding.

Fig. 6 (B) Forming ^{metal} vias in polymer by casting (ie doctor blading).





Side view FIG 7A



Top view FIG 7B

Figure 7. Arrangement for stacking, alignment and clamping of substrate layers for subsequent solder joining.

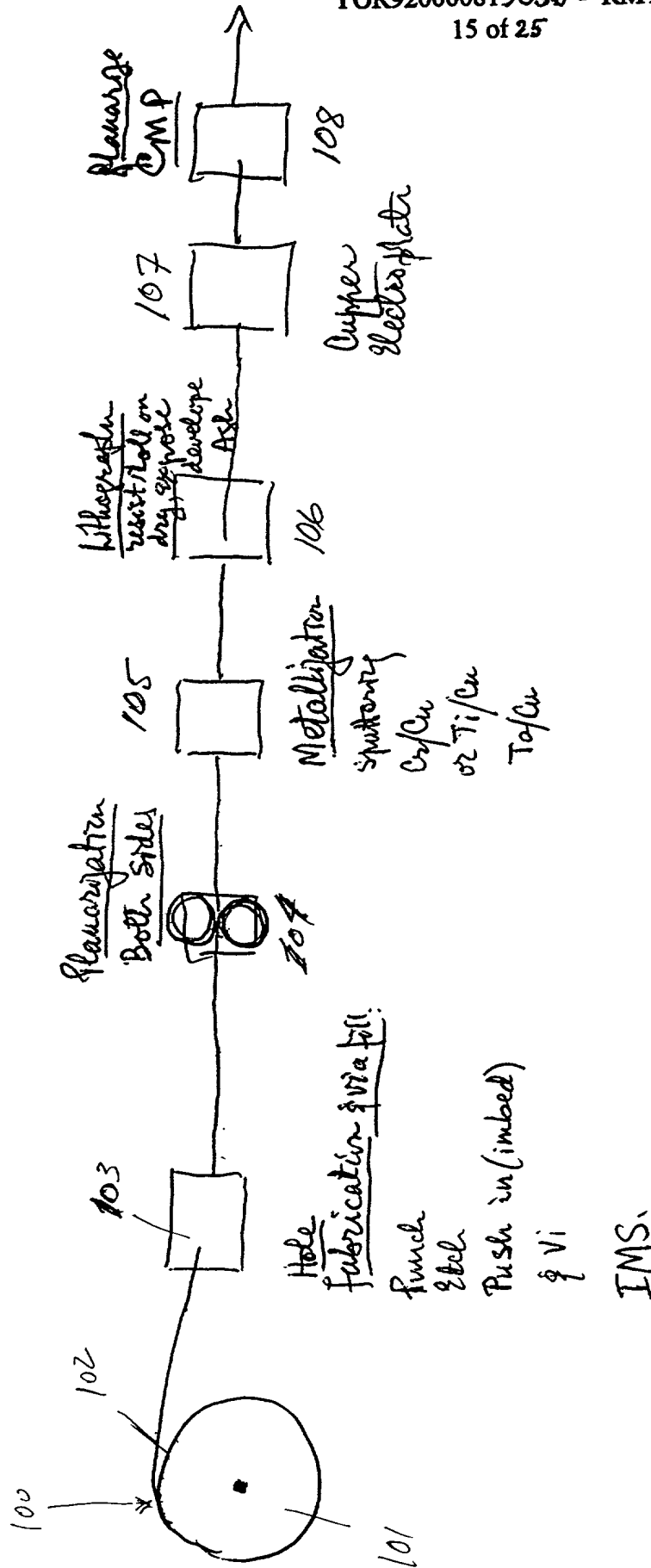


Figure. 8 A continuous fabrication process for individual layers comprising the display.

The flowchart illustrates the manufacturing process for a multi-layer printed circuit board (PCB) in 12 steps:

- 109**: Initial blank board.
- 110**: Remove resist and seed layer.
- 111**: Apply S18 dielectric.
- 112**: Flamurage to open Copper.
- 113**: Expose and Developed Ash.
- 114**: Electrodes Plate Co (S18) Immersion Plate Au.
- 115**: Cut.
- 116**: Seal.
- 117**: Align all individual layers clamp.
- 118**: Heat in.
- 119**: Fill individual layers with Electroplating fluid or LC.
- 120**: Seal.

```

graph TD
    117[117. Align all individual layers  
(clamped)] --> 118[118. Heat in vacuum & Solder]
  
```

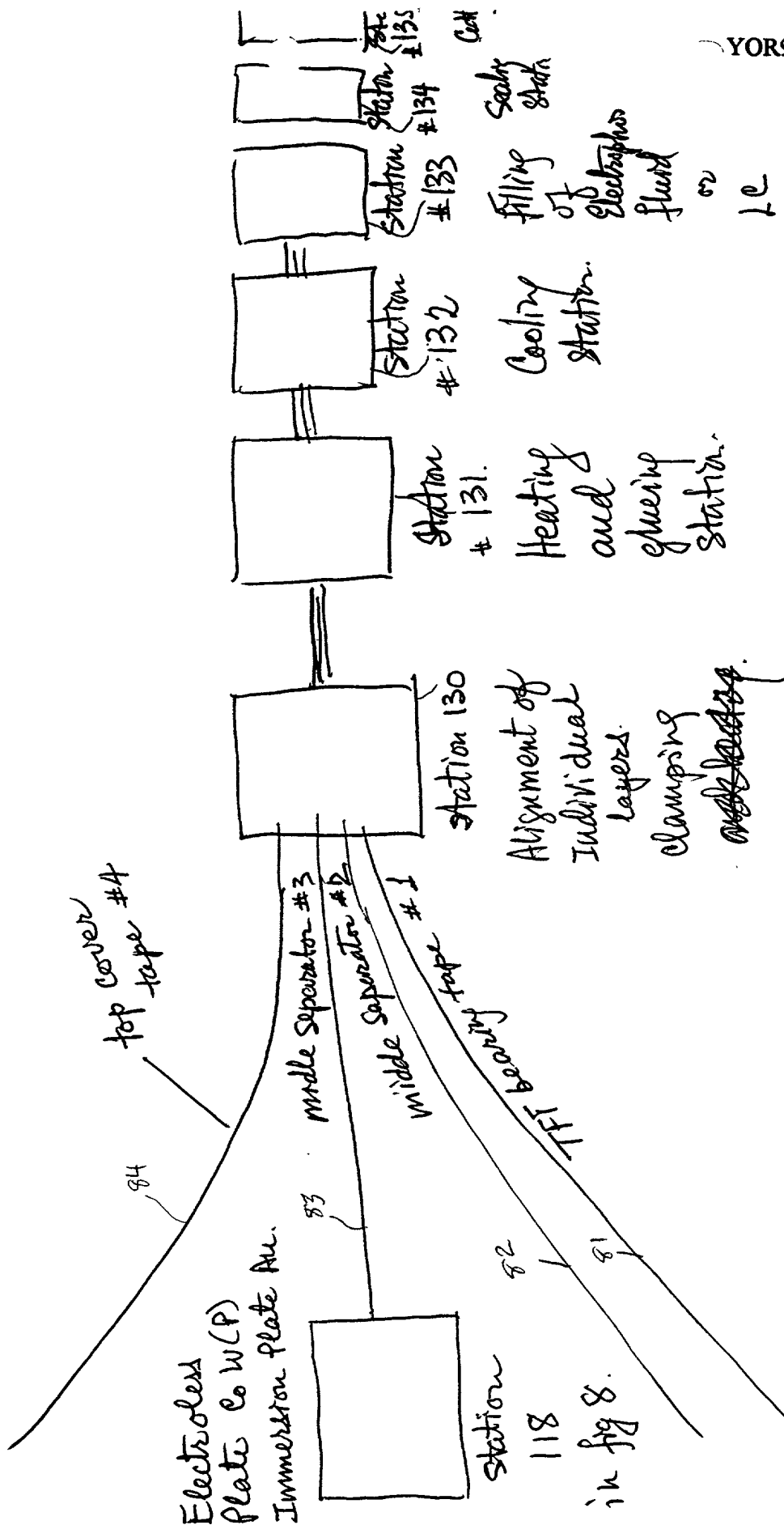
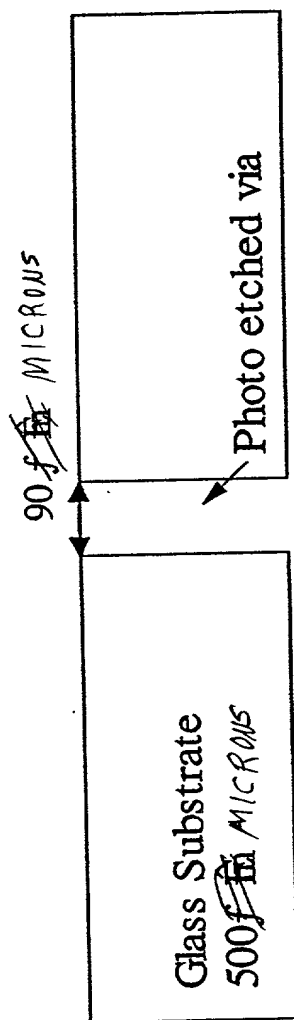



Figure 9.

Via and ITO

- 1. Via making by photo etching



- 2. Sputtering ITO and patterning

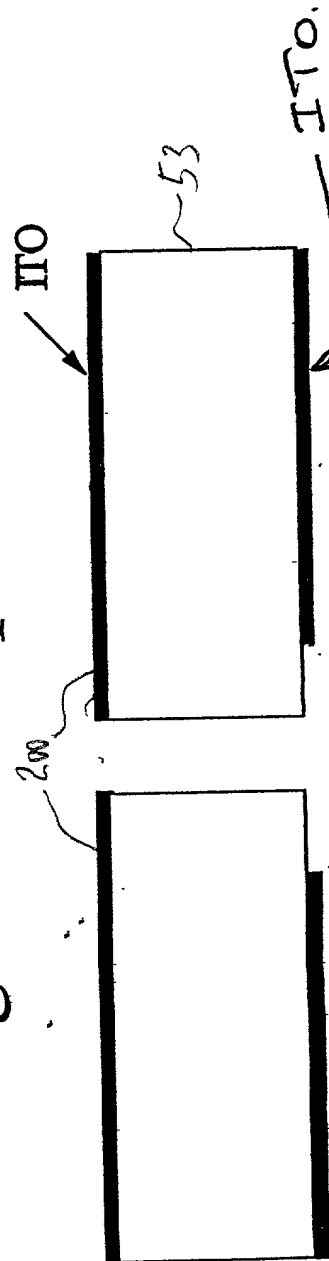


Figure 10(A) Fabrication of a guest-host liquid crystal Display.

Color Display: Vertical electrode

- 3. Vertical electrode by copper plating

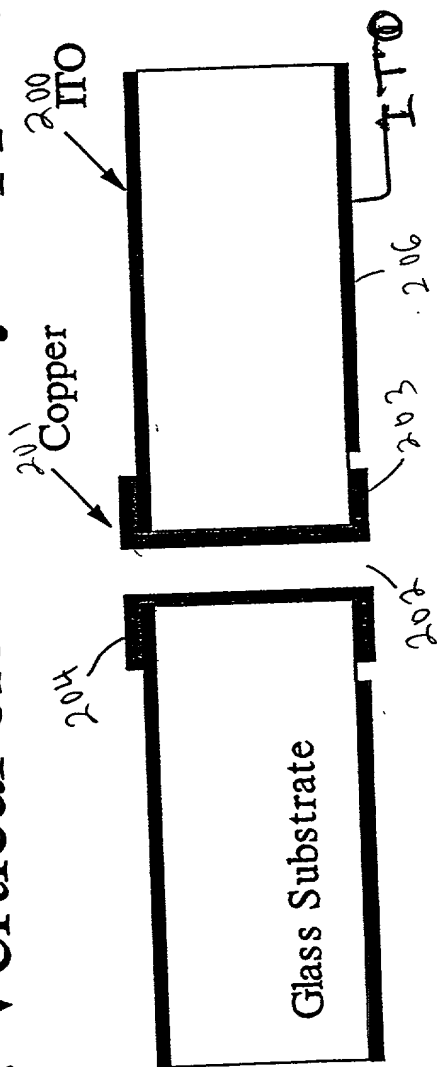


TABLE I

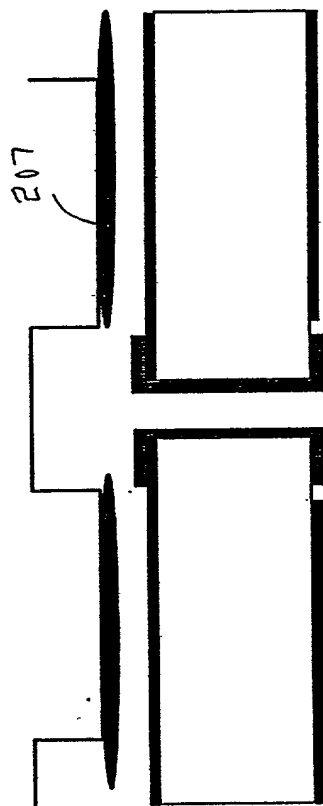
Substrate thickness (microns)	Via diameter (microns)	Aperture ratio (%) (3 vias in 300 microns pixel)
500	90	79
200	36	97
100	18	99

Figure 10B) Fabrication of through hole vias connected to ITO electrodes

Color Display: Polyimide coat

• 4. Polyimide coat and patterning

– Printing



~~– Laser ablation~~

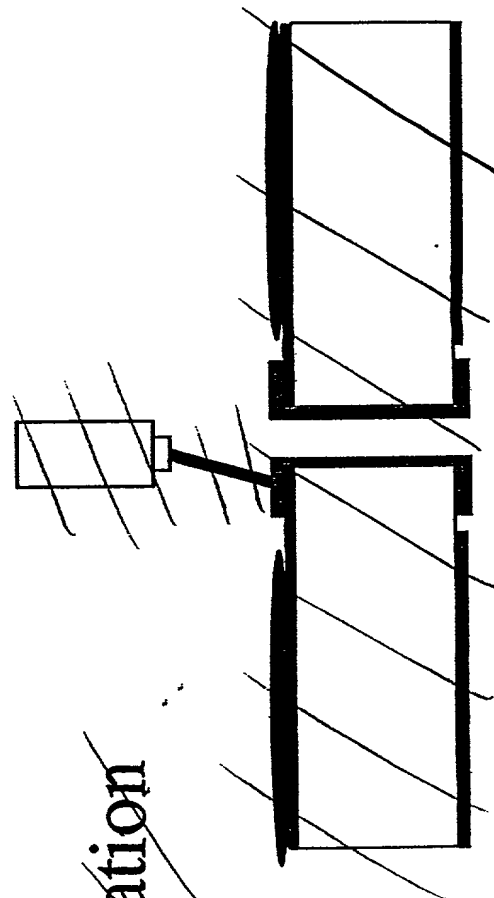


Figure ~~10(a)~~ 10(c)

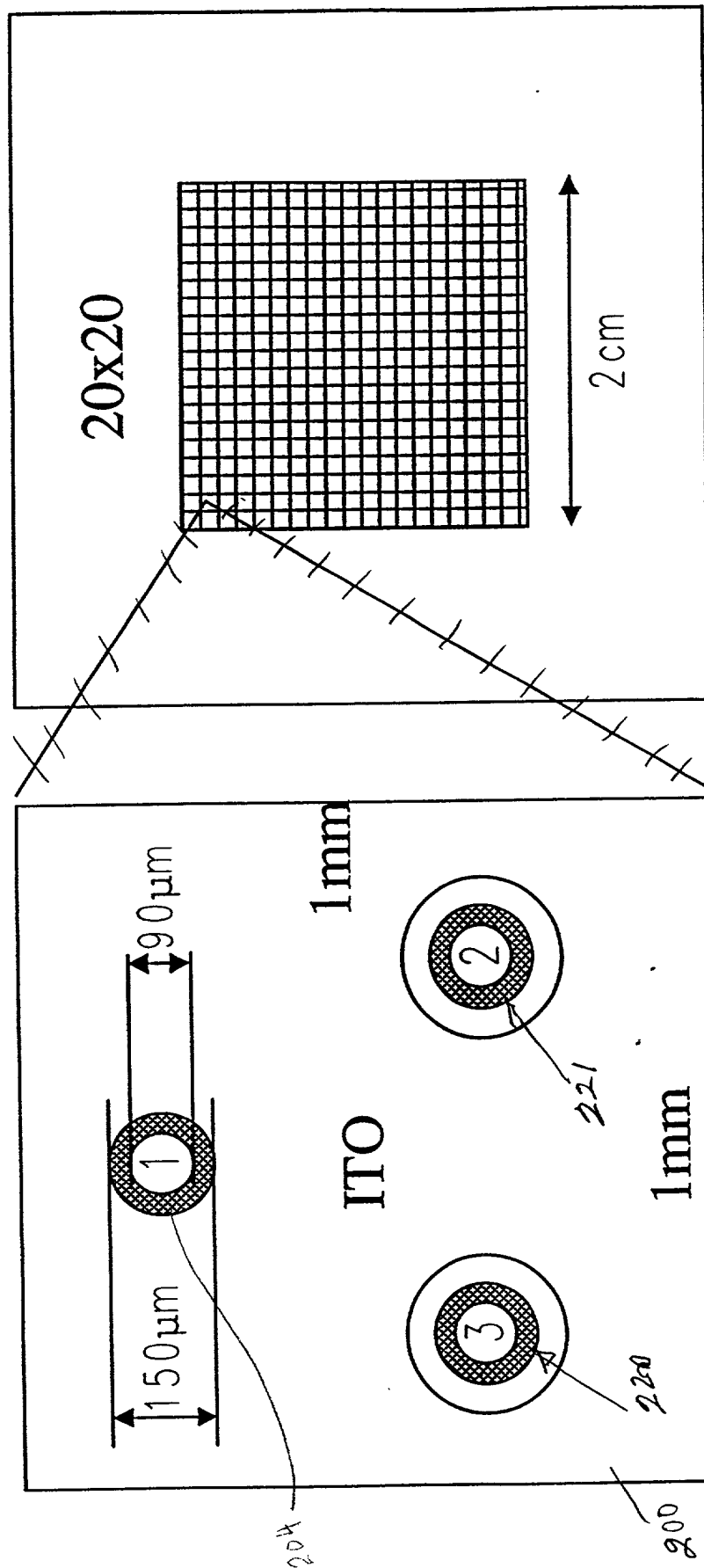
[illegible]

-
- Au
 Co/W(P)
 Cu
 210
 211
 207
 206
 208
 Polyimide
 ITO
 Copper
 Pb/Sn solder
 212

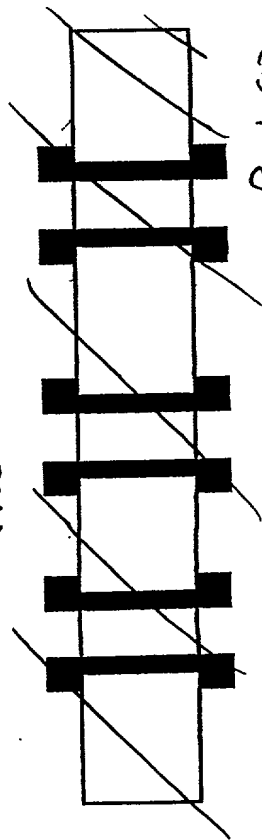
Figure 10(D) Preparation of two layers for via joining
The height of the flanges defines separation between layers

Color Display: Pixel Structure

and ITO



One Pixel



4 cm

(E) 10(F)

10 (E) Overall view first level electrical connections of metallized via to ITO.
Post (1) mounted Post (3) and (3) is isolated.

Pixel Structure

- Stacked Structure
 - Vertical electrode
 - Vertical electrical connection

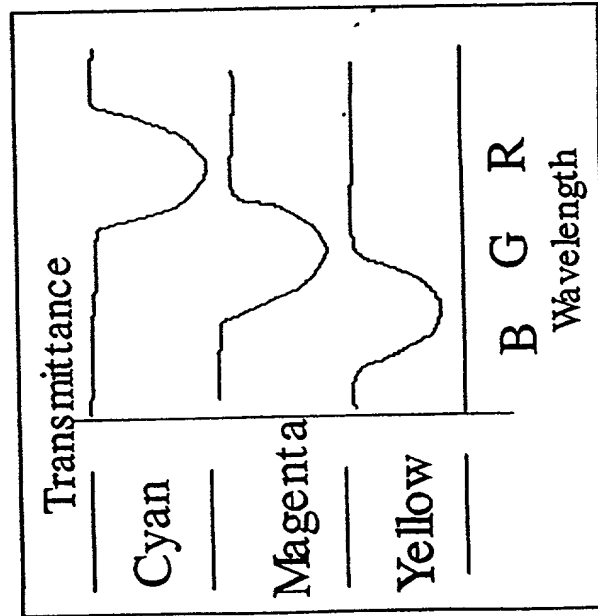


FIG 10F

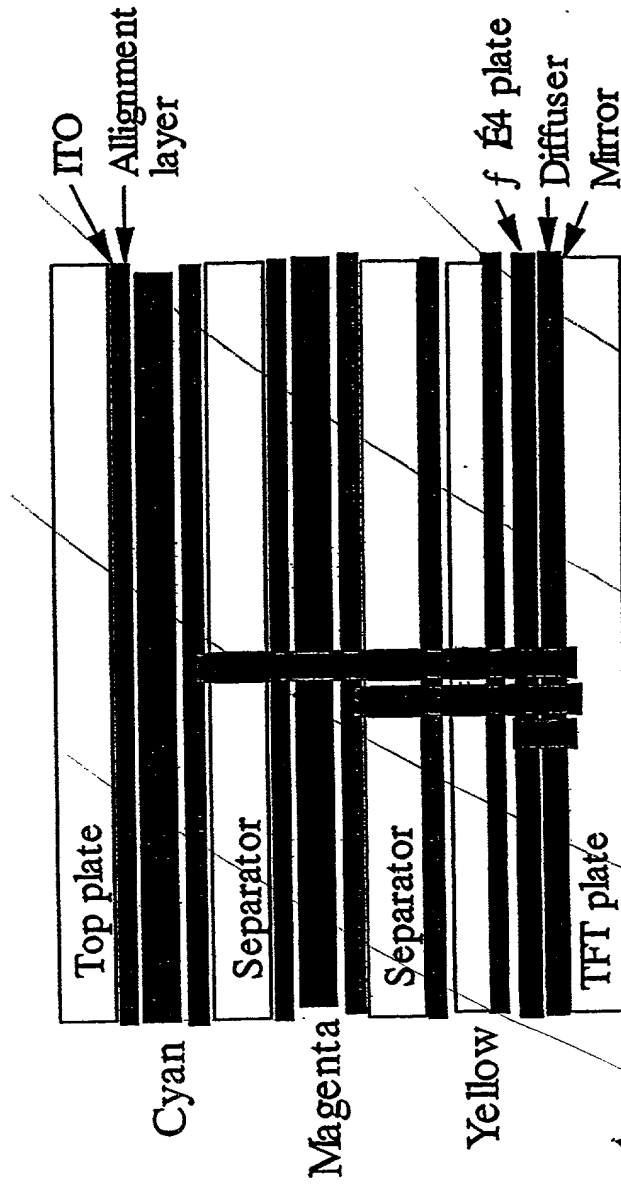
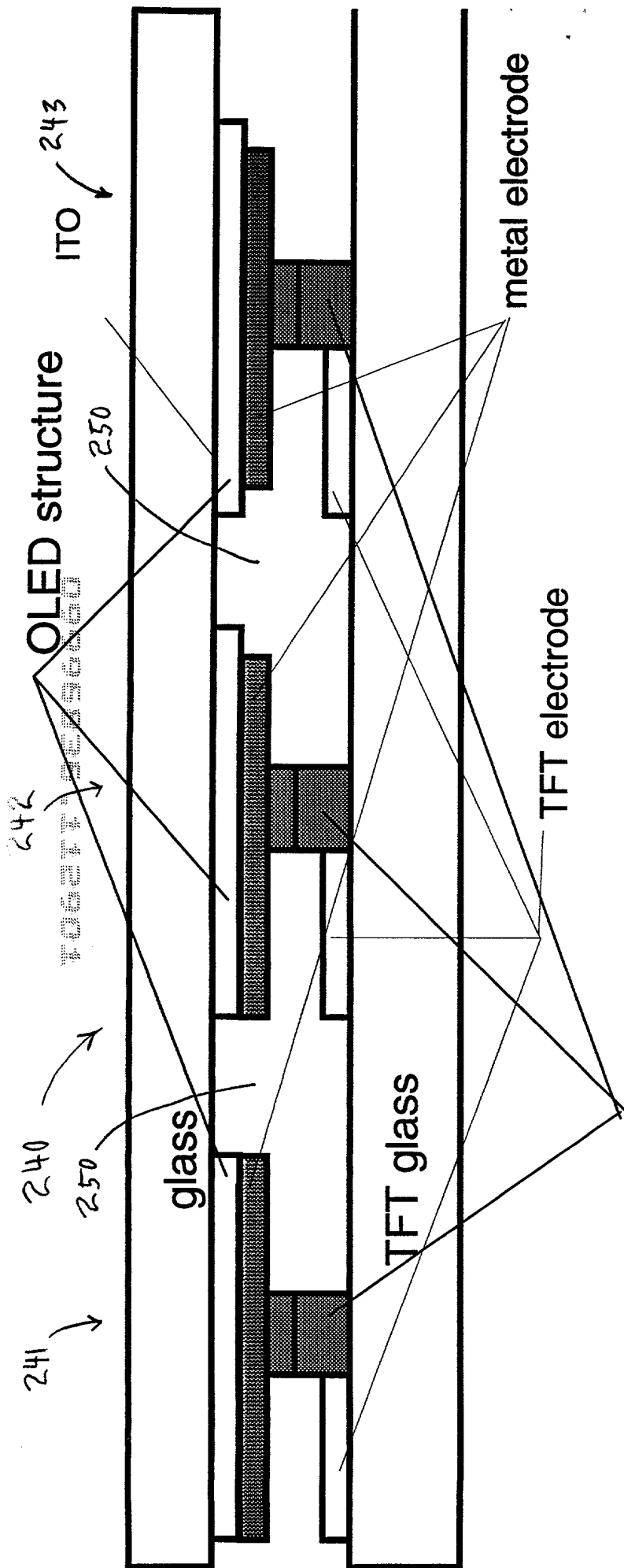


FIG 10F
Completed structure after joining.
(GH-LC Display)



Organic light emitting diode display (Bottom emission structure)

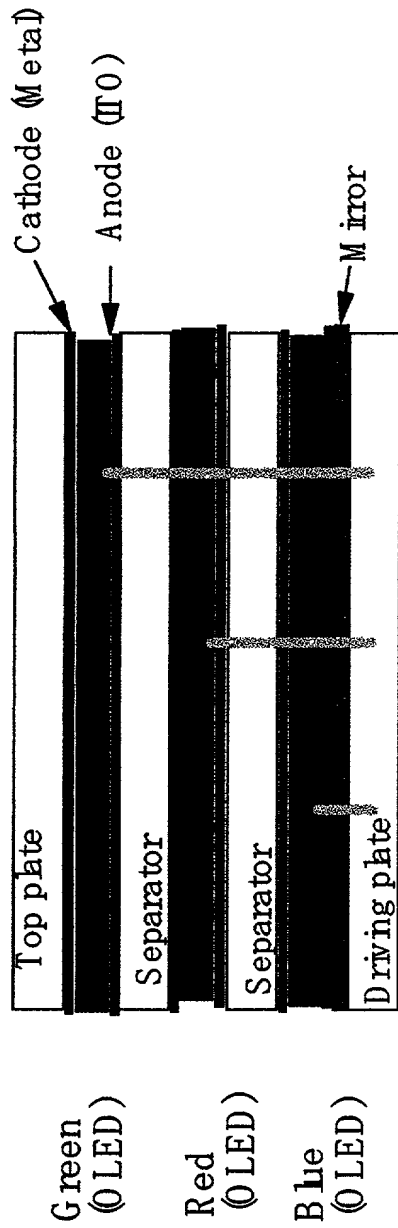


FIG 12

Three-layer stacked OLED